Article

Sliding ferroelectric memories and synapses based on rhombohedral-stacked bilayer MoS$_2$

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Recent advances have uncovered an exotic sliding ferroelectric mechanism, which endows to design atomically thin ferroelectrics from non-ferroelectric parent monolayers. Although notable progress has been witnessed in understanding the fundamental properties, functional devices based on sliding ferroelectrics remain elusive. Here, we demonstrate the rewritable, non-volatile memories at room-temperature with a two-dimensional (2D) sliding ferroelectric semiconductor of rhombohedral-stacked bilayer MoS$_2$. The 2D sliding ferroelectric memories (SFeMs) show superior performances with a large memory window of >8 V, a high conductance ratio of above 10^6, a long retention time of >10 years, and a programming endurance greater than 10^4 cycles. Remarkably, flexible SFeMs are achieved with state-of-the-art performances competitive to their rigid counterparts and maintain their performances post bending over 10^3 cycles. Furthermore, synapse-specific Hebbian forms of plasticity and image recognition with a high accuracy of 97.81% are demonstrated based on flexible SFeMs.

A ferroelectric is a polar material that features spontaneous charge polarization with two or more preferred stable polarization states, determined by its lattice symmetry breaking[1,2]. The ferroelectric polarization, which can be programmed (switched) via applying an external electrical field, is appealing for a myriad of technological advances and functionalities, including but not limited to ultra-dense random-access memories, in-memory computing to break today's von Neumann bottleneck, negative capacitance transistors to beat the "Boltzmann Tyranny", photovoltaic devices beyond the Shockley–Queisser limit, and artificial neurons for spiking neural networks[1,3–10].

Triggered by the growing technological demands of continued device downscaling and emerging data-centric applications, ferroelectricity down to atomically thin limit has become highly sought-after, but is challenging to obtain in conventional materials with three-dimensional (3D) lattices[5,6]. Two-dimensional (2D) layered materials knitted together by weak van der Waals (vdW) interactions provide an unprecedented platform for atomically thin ferroelectrics. In just a few

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years, we have had at our disposal dozens of 2D vdW ferroelectrics, such as $CuInP_2S_6$, In_2Se_3, WTe_2, and group-IV monochalcogenide monolayers[5,6,11–14]. Of particular interest, recent advances in 2D vdW ferroelectrics have uncovered a fundamentally new driving mechanism behind the spontaneous polarization schemes, i.e., sliding ferroelectrics[15–30]. Such exotic sliding ferroelectric mechanism enables the on-demand design of atomically thin ferroelectrics from non-ferroelectric parent monolayers, which can not only significantly broaden the range of available 2D ferroelectric materials (such as the scarce ferroelectric semiconductors), but also potentially outline a bright vision for a broad portfolio of emerging technological innovations. Although notable progress in 2D sliding ferroelectrics has been witnessed over the past few years, most studies are focused on identifying the presence of sliding ferroelectricity. Achieving functional sliding ferroelectric devices with competitive performances, which lays a strong foundation for 2D sliding ferroelectrics to fit into practical applications, is promising on the horizon yet remains elusive.

Here, we report the sliding ferroelectric field-effect transistors (FETs) at room temperature in which a 2D sliding ferroelectric semiconductor of rhombohedral-stacked (R-stacked) bilayer MoS_2 grown by a stacking-controlled technique is employed as the channel material. The fabricated sliding ferroelectric transistors at thicknesses of only two atomic layers exhibit rewritable, non-volatile memory behaviors with excellent performances, including a large memory window of >8 V, a high on/off conductance ratio of ~10^7, a long retention time of >10 years, and a programming endurance of over 10^4 cycles. Importantly, flexible sliding ferroelectric memories (SFeMs) are achieved with state-of-the-art performances competitive to their rigid counterparts and can be bent more than 10^3 times without degrading device performances. Further, flexible electronic synapses which enable the emulation of specific Hebbian forms of plasticity, such as long-term potentiation and depression, are demonstrated with sliding ferroelectric bilayer MoS_2 transistors. Finally, we construct a five-layer convolutional neural network (CNN) based on flexible sliding ferroelectric synapses and achieve an accuracy as high as 97.81% in the recognition of Modified National Institute of Standards and Technology (MNIST) handwritten-digit images.

Results
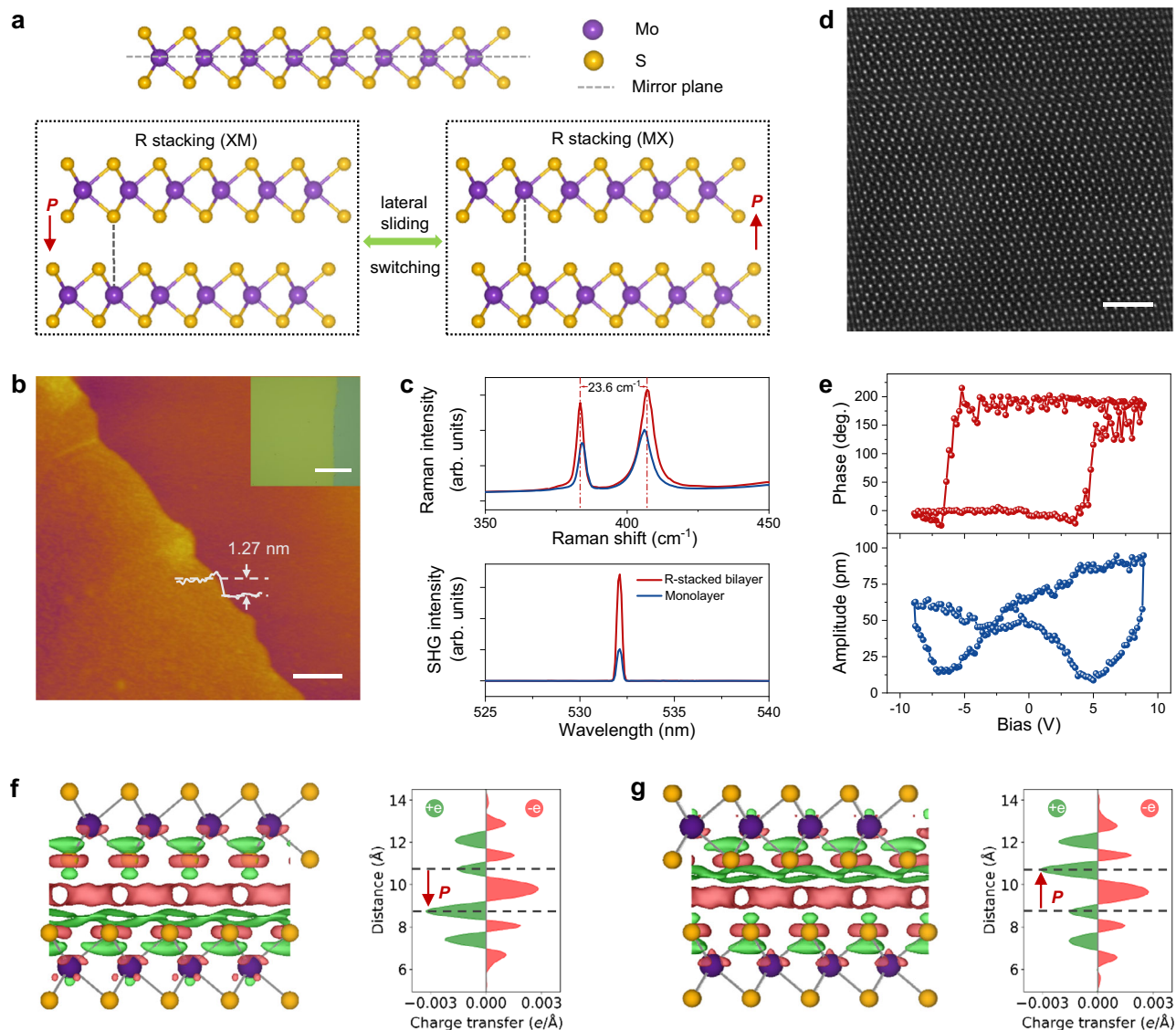
Sliding ferroelectrics of R-stacked bilayer MoS_2

Monolayer MoS_2, one of the most promising 2D semiconductors, holds great prospects for next-generation integrated circuits and flexible electronics because of its high intrinsic carrier mobility, excellent gate controllability, high on/off current ratio, ultra-low standby power, and remarkable flexibility[31–35]. Although inversion symmetry is intrinsically broken, monolayer MoS_2 (point group D_{3h}) is non-ferroelectric because of the out-of-plane mirror symmetry (upper panel of Fig. 1a). Remarkably, by stacking two MoS_2 monolayers in a parallel manner but with a lateral shift of one-third of the unit cell along the armchair direction, a R-stacked bilayer structure (polar point group C_{3v}) emerges, which breaks both the inversion and out-of-plane mirror symmetries (lower panel of Fig. 1a). This enables the generation of a spontaneous out-of-plane charge polarization from a general symmetry-breaking standpoint[2]. In addition, the R-stacked bilayer MoS_2 features two energy-degenerate stacking configurations, i.e., XM (MX) stacking order corresponding to the vertical alignment of chalcogen atoms in the top layer with molybdenum atoms in the bottom layer (and vice versa). Because such two stacking configurations can be viewed as mirror images of each other, their corresponding electric polarizations are opposite. Consequently, swapping the stacking configurations from one to another by an in-plane shear motion could result in the switching of spontaneous out-of-plane polarization and therefore exotic sliding ferroelectricity (lower panel of Fig. 1a).

Previously, the presence of sliding ferroelectric polarization in R-stacked bilayer MoS_2 has been demonstrated in micron-scale

samples obtained by direct mechanical exfoliation or assembled by the tear and stamp technique[19,20,22,23,36,37]. Here we employ inch-scale R-stacked bilayer MoS_2 grown by an interfacial epitaxy methodology (please refer to section "Methods" for more details)[38]. Inset of Fig. 1b displays the optical microscopy image of R-stacked bilayer MoS_2 transferred onto a silicon substrate with 20 nm Al_2O_3 dielectric layer for device fabrication which we shall come to shortly. Apparently, the transferred sample is quite uniform and clean, devoid of crackles and bubbles. The height image obtained from a tapping mode atomic force microscopy (AFM) is presented in Fig. 1b. The height line scan profile indicates that the thickness of MoS_2 is ~1.27 nm, providing a fingerprint of the bilayer nature. This is further corroborated through Raman spectra with a larger frequency difference between E_{2g} and A_{1g} phonon modes in bilayers, i.e., ~23.6 cm^{-1}, than that in monolayers, i.e., ~21.8 cm^{-1} (top panel, Fig. 1c)[39].

To verify that our bilayer MoS_2 belongs to R-stacking phase with sliding ferroelectricity rather than the trivial centrosymmetric 2H-stacking structure, we perform optical second harmonic generation (SHG) measurements (bottom panel of Fig. 1c). The SHG intensity of our bilayer sample is around four times that of monolayer. This largely evidences the R-stacking configuration given that the SHG efficiency from R-stacked MoS_2 shows a quadratic dependence on the layer number as a result of atomically phase-matched conditions[40,41]. By contrast, the SHG response of 2H-stacked bilayer MoS_2 would vanish due to the existence of inversion symmetry. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) is employed to further examine the stacking order. Atomic-resolution HAADF-STEM images (Fig. 1d and Supplementary Fig. 1) show that atoms are located not only at the corners of honeycomb lattice, but also at its center. This matches well with the R-stacked bilayer structure, but is incompatible with the 2H phase where atoms are located only at the corners of hexagonal lattice (Supplementary Fig. 2). We highlight that our samples are pure R-stacked bilayers (Supplementary Fig. 3), in stark contrast to a recent study in which R-stacked bilayer MoS_2 domains are only a small percentage and embedded in a highly dislocated and unstable non-ferroelectric matrix[42].

Having identified the R-stacked bilayer structure, we then perform piezoresponse force microscopy (PFM) measurements in the DART-SS-PFM mode to investigate the sliding ferroelectric behavior and spontaneous charge polarization switching. Figure 1e displays the off-field PFM phase (top panel) and amplitude (bottom panel) against the constant-voltage bias for an as-grown R-stacked bilayer MoS_2 directly on the metal substrate. The PFM amplitude exhibits a characteristic butterfly loop, while the corresponding PFM phase shows a hysteresis loop with a phase switching of ~180° at the minima of the amplitude response, evidencing the electrically switchable polarization states and ferroelectric nature. The existence of ferroelectricity in pure R-stacked bilayer MoS_2 is highly consistent with the recent optical spectroscopy imaging results[36] and the observed ferroelectricity in untwisted, commensurate MoS_2/WS_2 heterobilayers[21]. To further verify the existence of ferroelectricity in R-stacked bilayer MoS_2, we perform ab initio density functional theory (DFT) calculations to extract the interfacial differential charge densities (DCD, a quantity measuring the charge variation at the interface) of the two energy-degenerate stacking configurations[21]. Left panel of Fig. 1f, g presents the calculated interfacial DCD for XM (MX) stacking order. The separation of the electron accumulation (rose red) and the electron depletion regions (green) illustrates the explicit charge redistribution between the top and bottom layers. Their line profiles (right panels of Fig. 1f, g) unequivocally show the spontaneous out-of-plane electric polarization at the interfaces and its dipole direction can be programmed by switching the stacking configurations from one to another through a 1.23 Å lateral sliding along the armchair direction.

Fig. 1 | Sliding ferroelectricity of R-stacked bilayer MoS₂. a Cross-section view along the armchair direction of monolayer MoS₂ (top) and R-stacked bilayer MoS₂ (bottom). R-stacked bilayer MoS₂ features two energy-degenerate stacking configurations, i.e., XM (MX) stacking order corresponding to the vertical alignment of sulfide atoms in the top layer with molybdenum atoms in the bottom layer (and vice versa). **b** AFM height image of R-stacked bilayer MoS₂ showing thickness of around 1.27 nm; scale bar 500 nm. Inset: optical image of R-stacked bilayer MoS₂ after transferring onto a silicon substrate coated with 20 nm Al₂O₃; scale bar 200 μm.

c Raman (up) and SHG spectra (bottom) of monolayer (light blue) and R-stacked bilayer MoS₂ (red). **d** Atomic-resolution HAADF-STEM image of R-stacked bilayer MoS₂. Scale bar, 2 nm. **e** Off-field PFM phase (top) and amplitude (bottom) of an as-grown R-stacked bilayer MoS₂ against the constant-voltage bias directly on the metal substrate, showing the typical ferroelectric hysteresis and butterfly loop, respectively. **f, g** Interlayer charge density distributions (left) and their corresponding line profiles along z direction (right) for XM (**f**) and MX stacking orders (**g**), indicating opposite ferroelectric polarization between them.

Sliding ferroelectric memory

R-stacked bilayer MoS₂ is expected to be an exotic sliding ferroelectric semiconductor integrating the superior transistor performances of non-ferroelectric monolayer MoS₂ and robust ferroelectric properties designed from sliding mechanism, and thus holds great promise for emerging technological applications such as non-volatile memories, neuromorphic computing, and brain-inspired intelligent devices[7,43,44]. To demonstrate such potentials, we first fabricate sliding ferroelectric FET devices utilizing R-stacked bilayer MoS₂ as the channel material. Benefitting from the large-scale R-stacked bilayer MoS₂ afforded by the direct growth method, the batch fabrication of sliding ferroelectric FET arrays over several millimeters is realized (left panel of Fig. 2a; section "Methods" provides the fabrication details). Right panel of Fig. 2a illustrates the device geometry with Ti–Au–Ti as the local back-gate electrode, 20-nm Al₂O₃ as the dielectric layer, and R-stacked

bilayer MoS₂ as the ferroelectric semiconductor channel. Semimetallic Sb is chosen as the source/drain electrodes to suppress Fermi-level pinning and reduce contact resistance (Supplementary Note 2)[45]. Unless otherwise specified, all electrical measurements in the main text are performed at room temperature with an Agilent semiconductor parameter analyzer under a base pressure of 10^{-6} Torr.

Figure 2b plots the output characteristic curves of a representative R-stacked bilayer MoS₂ FET device under different back-gate voltages V_{GS} (sweeping from 0 V to 10 V with a step of 1 V). The overall linear output characteristics suggest the low-resistance Ohmic contact behavior. Figure 2c presents the double-sweep transfer characteristics of a typical R-stacked bilayer MoS₂ FET device by scanning the back-gate V_{GS} from −10 V to +10 V and then back to −10 V at a fixed drain voltage V_{DS} = 1 V. The R-stacked bilayer MoS₂ FET shows a typical n-type semiconducting characteristic with a high on/off current ratio of
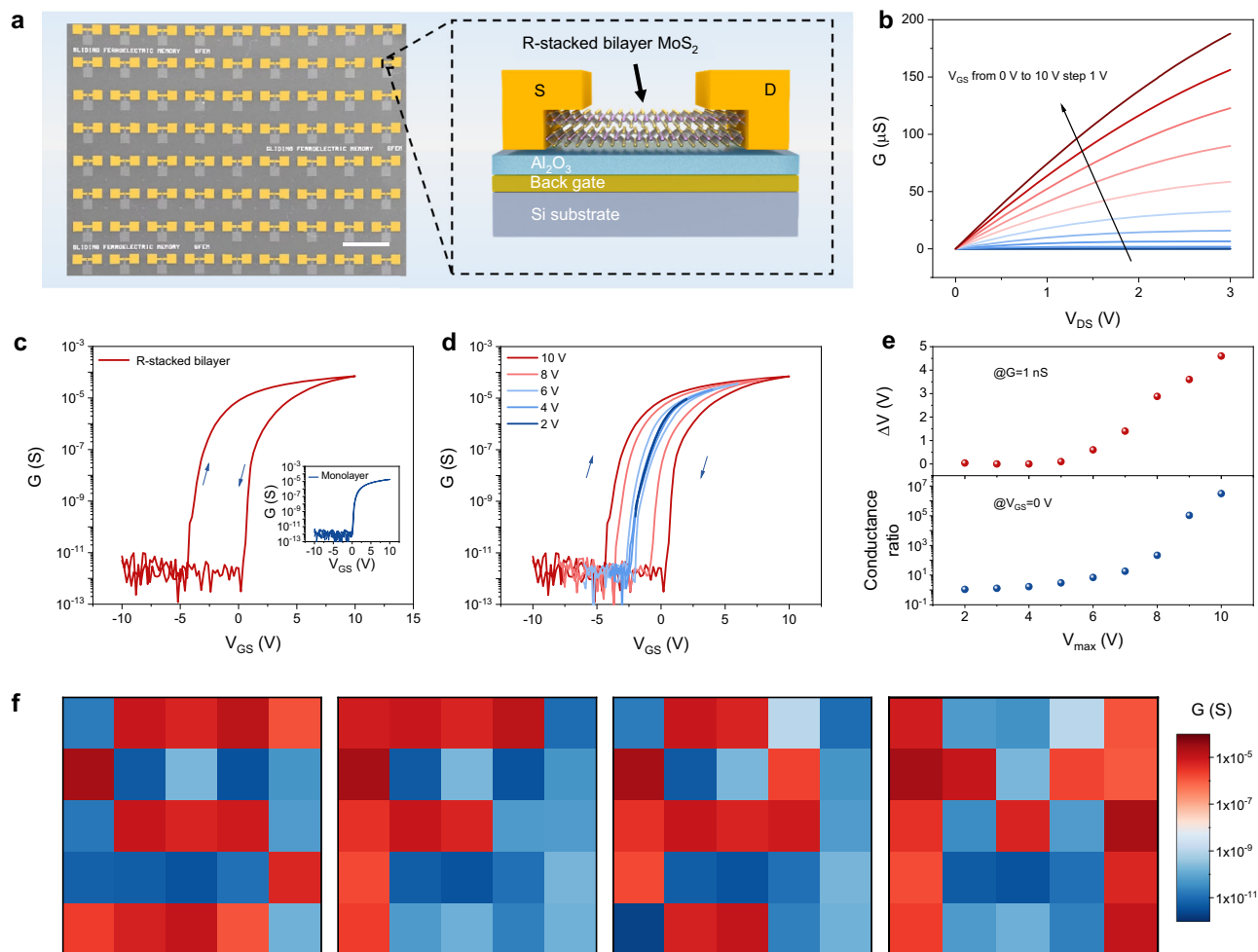
Fig. 2 | Sliding ferroelectric memory on rigid substrate. a Left: false color scanning electron microscopy image of sliding ferroelectric FET arrays. Scale bar, 500 μm. Right: schematic of the device structure which consists of rigid silicon substrate, local metal gate, 20 nm Al_2O_3 dielectric insulator, R-stacked bilayer MoS_2 channel, and metal contacts. **b, c** Output (**b**) and dual-sweep transfer characteristic curves (**c**) of a R-stacked bilayer MoS_2 device. Inset in (**c**) is the transfer curves of a monolayer MoS_2 device. **d** Dual-sweep transfer curves of R-stacked bilayer MoS_2 devices with different scanning voltages. The scan rate is 200 mV/s. **e** Hysteresis memory window at $G = 1$ nS (top) and conductance ratio at $V_{GS} = 0$ V (bottom) as a function of the sweeping voltages. **f** Color maps of conductance for a 5×5 R-stacked bilayer MoS_2 FET arrays recorded at $V_{DS} = 1$ V and $V_{GS} = 0$. By programming the sliding ferroelectric polarization states with a gate voltage of +10 V (i.e., HRS) or −10 V (i.e., LRS), non-volatile memory maps with the characters "S", "F", "e", and "M" are achieved.

~5×10^7. Remarkably, a prominent clockwise hysteresis loop is observed. To confirm that the observed hysteresis loop is from the switching of sliding ferroelectric polarization rather than from extrinsic origins such as trapped charges at the interface, we fabricate non-ferroelectric monolayer MoS_2 FET devices adopting exactly the same device geometry and manufacturing process. Inset of Fig. 2c and Supplementary Fig. 5 plot the bidirectional scanning transfer curves of monolayer MoS_2 devices. The hysteresis is negligible for all non-ferroelectric monolayer MoS_2 FETs when the gate voltage is scanned in a closed loop between −10 and +10 V (more than 20 devices are measured). The strong contrast between the results of non-ferroelectric monolayer and ferroelectric bilayer MoS_2 provides the smoking gun evidence that the observed hysteresis windows in R-stacked bilayer MoS_2 originate from the ferroelectric polarization switching. We highlight that the observed clockwise hysteresis loop of R-stacked bilayer MoS_2 can be understood as when the ferroelectric semiconductor of R-stacked bilayer MoS_2 is in the polarization down state, ferroelectric dipole moment would lead to the redistribution of the mobile carriers (electrons for *n*-type MoS_2) and thus bends the electron band downwards (upper panel, Supplementary Fig. 8). This increases the carrier density in the transistor channel and gives rise to the low-resistance state (LRS). In stark contrast, when R-stacked bilayer

MoS_2 is in the ferroelectric polarization upstate, the electron band upwards and therefore the channel carrier density is depleted (lower panel, Supplementary Fig. 8), resulting in the high resistance state (HRS). Therefore, the switch of ferroelectric polarization using the gate voltage (V_{GS}) causes a prominent clockwise hysteresis loop and the ferroelectric FETs are alternatively operated between the on and off states via gating control. It is noteworthy that similar results with clockwise hysteresis loop have been observed previously for 2D ferroelectric In_2Se_3-based transistors[46].

Figure 2d displays the bidirectional scanning transfer curves of an R-stacked bilayer MoS_2 FET device under different V_{GS} sweeping ranges, where the V_{DS} is fixed at 1 V. The extracted hysteresis memory window (ΔV) at $G = 1$ nS against the applied maximum gate voltage (V_{max}) is presented in the top panel of Fig. 2e. Obviously, no noticeable hysteresis window is observed when the V_{max} is less than 4 V. This is highly consistent with the ferroelectric feature that the switching of polarization state typically requires a critical electric field. When the V_{max} is ≥4 V (the corresponding critical electrical field is -0.2 V/nm, close to the previously reported results[20]), the hysteresis window becomes larger as the sweeping range V_{GS} increases. This indicates that the ferroelectric polarization can be precisely programmed by the applied electric fields, facilitating multiple independent drain-to-

source conductance states for electronic synapses as will be shown in latter discussions. A large hysteresis memory window of ~4.6 V is obtained under a V_{GS} sweep range of ±10 V. It is noteworthy that the memory window can be further enlarged by increasing the thickness or lowering the dielectric constant of dielectric layer, but this will inevitably lead to an increase in power consumption. Therefore, a trade-off between enlarged memory window and minimized power consumption is required based on the practical applications.

As a result of hysteresis, the R-stacked bilayer MoS_2 FET device exhibits two distinct resistance states at zero gate voltage ($V_{GS} = 0$), i.e., LRS and HRS. The conductance ratio between the two states versus V_{max} is depicted in the bottom panel of Fig. 2e. Apparently, when the applied V_{max} is larger than 4 V, the conductance ratio increases sharply with V_{max} and can reach up to ~8×10^6 under a V_{GS} sweeping range of ±10 V. The retention characteristics of R-stacked bilayer MoS_2 FET devices reveal that both the LRS and HRS do not show obvious degradation up to 10^3 s (Supplementary Fig. 10a), indicating stable non-volatile memory behavior. More remarkably, the extrapolation of data retention suggests that the LRS and HRS could be maintained for more than 10 years with a conductance ratio exceeding 10^6. Further, the programming endurance characteristics demonstrate that the R-stacked bilayer MoS_2 FET devices can survive over ~10^4 cycles without degradation (Supplementary Fig. 10b). The extrapolation of endurance indicates that negligible LRS and HRS degradation and a conductance ratio of above 10^6 can potentially be remained after 10^{13} switching cycles, which is adequate for memory applications and can even meet the requirement for edge (10^9) and cloud training (10^{12})[4,47]. Our SFeM integrates excellent retention time and superb programming endurance, promising the prospect of data-centric applications such as in-memory computing[4,47].

To evaluate the device uniformity, a 5×5 R-stacked bilayer MoS_2 FET array is tested. By programming the sliding ferroelectric polarization states with a gate voltage of +10 V (i.e., HRS) or −10 V (i.e., LRS), non-volatile memory maps with the characters "S", "F", "e" and "M" are achieved successfully by recording the conductivity at $V_{DS} = 1$ V and $V_{GS} = 0$ (Fig. 2f). The reprogrammable memory maps and strong conductance contrast between HRS (blue) and LRS (red) evidence superior device homogeneity.

Flexible sliding ferroelectric memory

Thanks to the 2D nature of only two atomic layers, R-stacked bilayer MoS_2 would not only harbor robust ferroelectric properties, but also show remarkable flexibility[31,32]. Consequently, R-stacked bilayer MoS_2 may offer unprecedented opportunities to implement flexible ferroelectric memory and thus promise the prospect of emerging portable, wearable, and implantable electronics[48]. We now pursue the fabrication of flexible non-volatile memory devices based on the sliding ferroelectric semiconductor of R-stacked bilayer MoS_2 in a back-gate geometry, where polyethylene terephthalate (PET) and 30-nm Al_2O_3 are employed as the substrate and dielectric layer, respectively (Fig. 3a). Figure 3b presents the dual-sweep $I_{DS}-V_{GS}$ transfer characteristics of a flexible R-stacked bilayer MoS_2 FET device under three different test conditions, i.e., the pristine flat state before bending (black), the bending state corresponding to a tensile strain of ~1.3% (red) and the post-bend flat state after 1000 consecutive cycles of bending test (blue). Apparently, the FET performances under these three test conditions such as on-off current ratio are essentially the same. This proves that R-stacked bilayer MoS_2 is remarkably flexible with an excellent tolerance to thousands of bending tests, facilitating the development of high-performance flexible devices.

Remarkably, a large hysteresis memory window ($\Delta V > 8$ V at $G = 1$ nS) with the non-volatile LRS and HRS at $V_{GS} = 0$ differing by more than six orders of magnitude, is observed for all the three test conditions (Fig. 3b). This bears striking resemblance to the results measured on rigid silicon substrate (Fig. 2). It is noteworthy that the hysteresis

memory window of flexible SFeM is larger than that of SFeM on rigid substrate under a same V_{GS} sweeping range of ±10 V (~4.6 V, top panel of Fig. 2e). This can be understood as that the thickness of Al_2O_3 dielectric layer is thicker for flexible SFeM (i.e., 30 and 20 nm for SFeM on flexible and rigid substrate, respectively). Figure 3c depicts the retention characteristics of a flexible SFeM, which is pre-programmed to the HRS (LRS) through a +10 V (−10 V) gate voltage pulse with width of 100 ms (left inset of Fig. 3c), and then read out via a 1 V source-drain bias under a floating gate configuration. For all the three configurations measured, no appreciable degradation is observed up to ~10^4 s for both the non-volatile LRS and HRS, offering the affirmative evidence of a long data retention time. Significantly, even after being subjected to 10^3 cycles of bending, we could still extrapolate the 10-year retention time for the flexible SFeM with a conductance ratio of ~10^6 between the LRS and HRS (inset of Fig. 3c).

To evaluate the endurance characteristics of flexible SFeM, we alternately apply programming gate voltage pulses of ±10 V (width, 100 ms; period, 500 ms, left inset of Fig. 3d), and monitor the HRS/LRS conductance at intervals of several cycles with a 1 V source-drain bias at $V_{GS} = 0$ (Fig. 3d). Remarkably, the flexible SFeM does not show noticeable degradation after ~10^4 cycles of ferroelectric switching (Fig. 3d and Supplementary Fig. 12b). More importantly, the projected endurance indicates that the non-volatile LRS and HRS, differing by a conductance ratio of above 10^6, can potentially maintain after 10^{13} programming cycles even after 10^3 cycles of bending (Supplementary Fig. 12b). The endurance of flexible SFeM against the bending cycles is also evaluated (inset of Fig. 3d). The negligible HRS and LRS degradation up to 1000 cycles of bending reveals the superior immunity to bending. This reinforces the robustness of sliding ferroelectricity in R-stacked bilayer MoS_2 and will boost technological applications in a series of flexible scenarios. We highlight that this is the first time, to the best of our knowledge, that flexible SFeM is constructed by employing ferroelectric semiconductor as the channel material.

To characterize the homogeneity, a 5×5 SFeM array is fabricated on flexible PET substrate. The conductances of the LRS and HRS of these 25 flexible SFeM devices after 1000 cycles of bending (the corresponding memory window and conductance ratio) are depicted in Fig. 3e (Fig. 3f), demonstrating good uniformity. Further, we benchmark the performances of our flexible SFeM. Overall, our flexible SFeM based on R-stacked bilayer MoS_2 shows competitive performances compared with their rigid counterparts, including a large memory window of >8 V, a high conductance ratio of above 10^6, a long retention time of >10 years, and a programming endurance greater than 10^4 cycles. Figure 3g and Supplementary Table 1 compare the characteristics of our flexible SFeM (i.e., memory window, retention, endurance, conductance ratio, flexibility, and thickness) with those of previously reported ferroelectric FET devices with 2D ferroelectric materials as the channel materials or non-ferroelectric 2D semiconductor/ferroelectric materials as the channel materials/gate insulators, showing that our flexible SFeM at thicknesses of only two atomic layers is very promising[7,43,44,49–51].

Flexible sliding ferroelectric synapses

Typically, in human neural networks, the transmission of nerve impulse signals from a pre-synaptic to a post-synaptic neuron as neurotransmitters diffuse through the synaptic cleft can be recognized by an excitatory/inhibitory post-synaptic current (PSC) (Fig. 4a). The ability to modulate the PSC amplitude (i.e., synaptic weight), which is believed to endow the brain with the ability to learn and process information, is referred to as synaptic plasticity[52,53]. Effective emulation of synaptic-like behavior in electronic devices, especially synaptic plasticity, would facilitate the development of energy-efficient brain-like neuromorphic computing to overcome the limitations of current von Neumann architectures in terms of energy consumption and throughput[4,52–57].
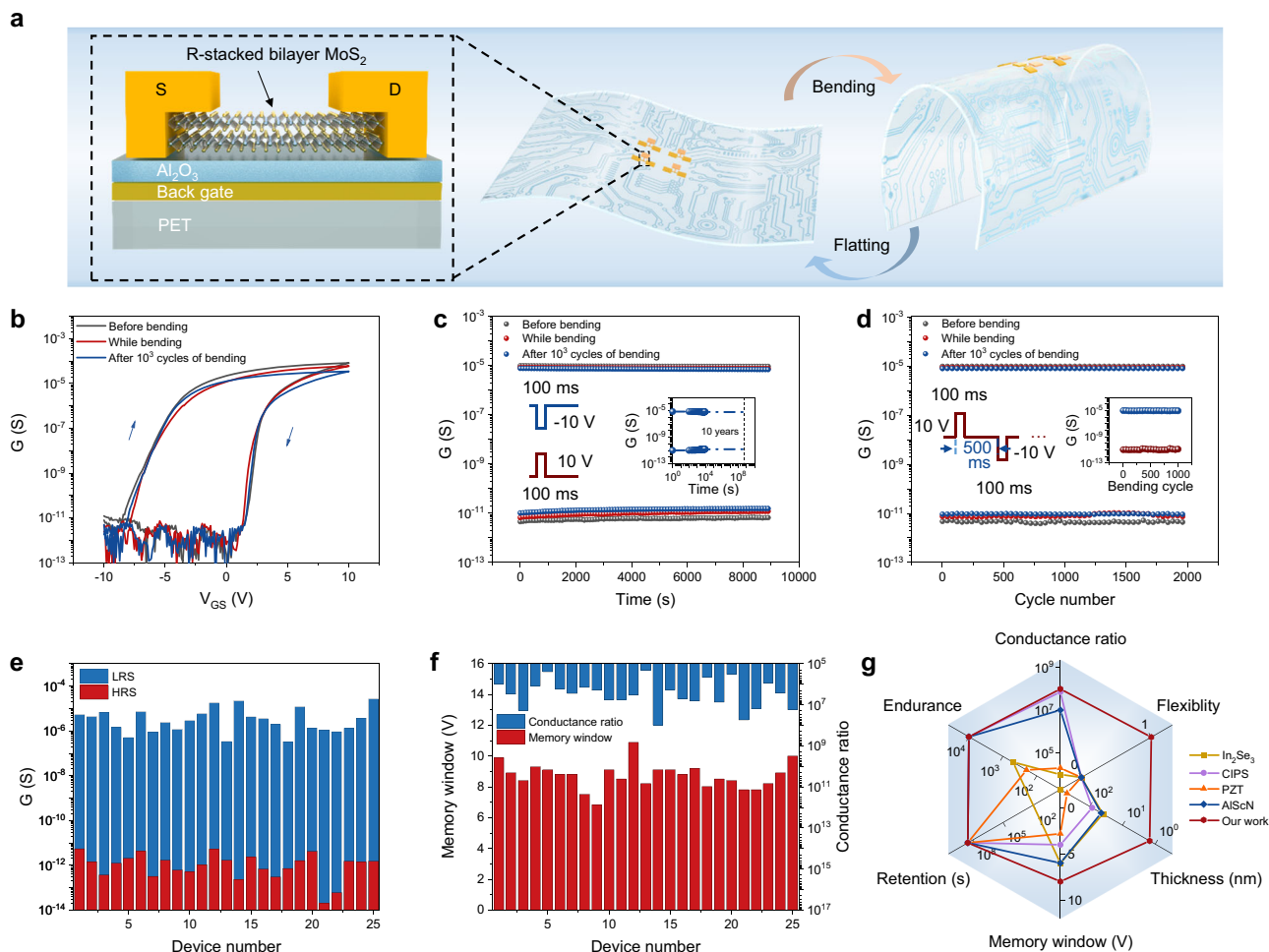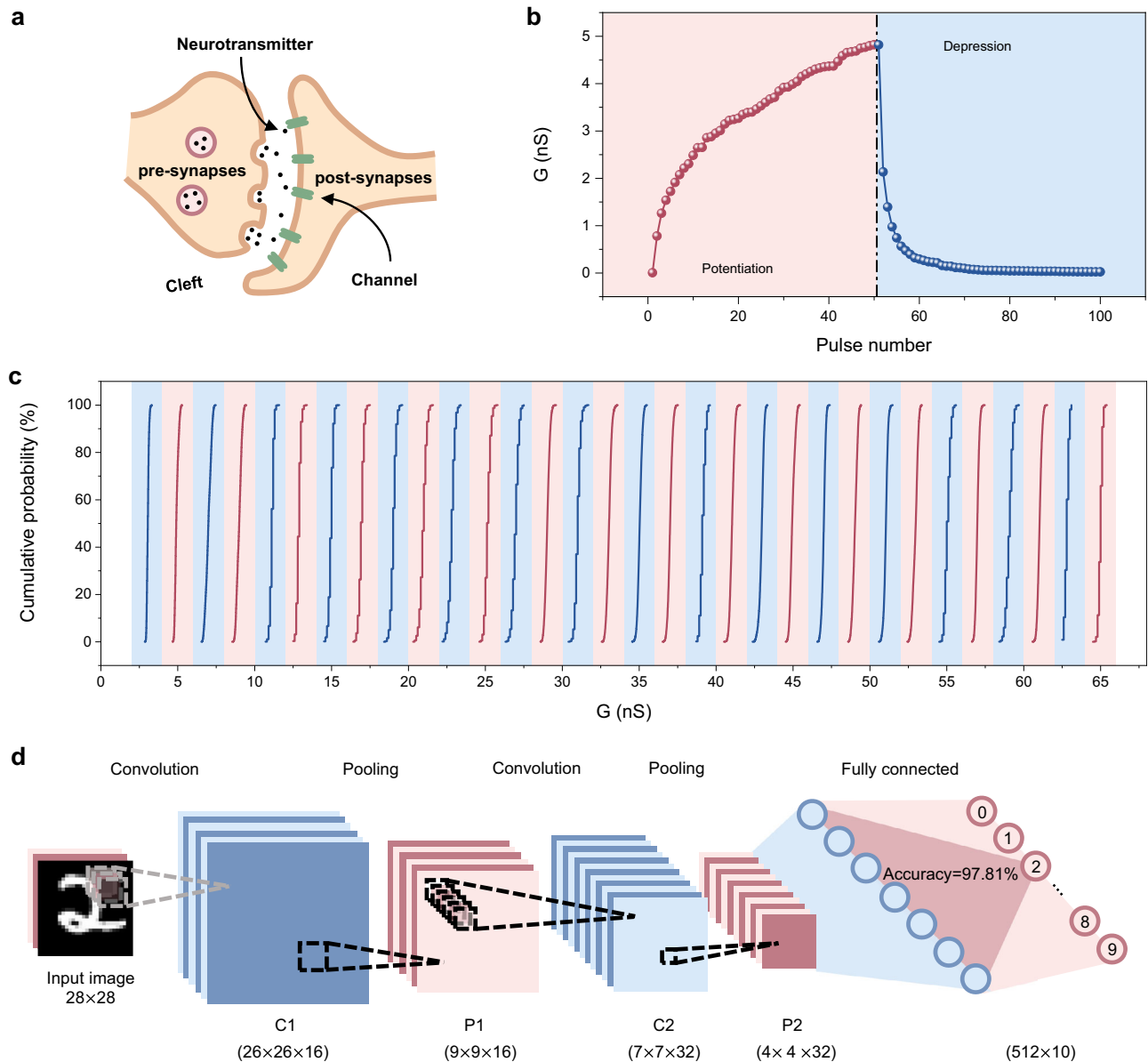
Fig. 3 | Flexible sliding ferroelectric memory. a Left: schematic of flexible SFeM device on PET substrate. Illustration of flexible SFeM under flat (middle) and bending states (right). **b** Transfer characteristic curves of flexible SFeM under different test conditions, i.e., the pristine flat state before bending (black), the bending state corresponding to a tensile strain of -1.3% (red) and the flat situation after 1000 consecutive cycles of bending test (blue). **c** Retention characteristics of a flexible SFeM, which is pre-programmed to the HRS (LRS) through a +10 V (−10 V) gate voltage pulse with width of 100 ms, and then read out via a 1 V source-drain bias at $V_{GS} = 0$. Inset: the extrapolation of the data retention indicates that the LRS and HRS could be maintained for more than 10 years with a conductance ratio exceeding 10^6

even after being subjected to 10^3 cycles of bending. **d** Endurance characteristics of a flexible SFeM. The programming gate voltage pulses are alternating +10 V and −10 V in amplitude and 100 ms in width. Inset: the endurance of a flexible SFeM against the bending cycle. **e**, **f** Statistical data of conductance of LRS/HRS (**e**) and conductance ratio/memory window (**f**) from 25 devices after 1000 cycles of bending. **g** Comparison of our flexible SFeM with previously reported ferroelectric FET devices with 2D ferroelectric materials as the channel materials or non-ferroelectric 2D semiconductor/ferroelectric materials as the channel materials/gate insulator[7,43,44,49–51]. CIPS: $CuInP_2S_6$; PZT: $Pb[Zr_{0.2}Ti_{0.8}]O_3$.

Given the precisely programmable ferroelectric polarization states, the flexible SFeM based on R-stacked bilayer MoS_2 shows highly controllable drain-to-source conductance states with the magnitude and width of the gate voltage pulse (Supplementary Figs. 14 and 15), and thus can operate as an extraordinary artificial synapse to emulate the plasticity learning rules of biological synapses, where gate voltage pulses simulate pre-synaptic input and channel conductance is identified as the synaptic weight. It is noteworthy that flexible electronic synapses down to 2D limit (i.e., <5 nm), which are in high demand for emerging wearable devices and edge intelligence devices, have not been implemented previously.

Figure 4b depicts the synaptic weight PSC of an SFeM on flexible PET substrate obtained by applying a gate voltage pulse sequence consisting of alternating 50 negative (−5 V, 15 ms) and 50 positive pulses (+5 V, 15 ms). Interestingly, via training with a consecutive negative (positive) gate pulse, the synaptic weight PSC increases (decreases) progressively, enabling the emulation of the long-term potentiation (long-term depression). Note that long-term potentiation and depression are two essential synapse-specific Hebbian forms of

plasticity that underlie training-based learning. To further demonstrate the neuromorphic computing of flexible SFeM, 32 independent drain-to-source conductance states are extracted (Fig. 4c). These conductance states are well separated and show good retention with no apparent degradation over time (Supplementary Fig. 16a), facilitating weight update and high accuracy. To this end, we construct a five-layer CNN based on flexible sliding ferroelectric synapses to execute the recognition of MNIST handwritten-digit images. Note that the dynamic conductance for CNN simulation is extracted from Fig. 4c and ranges from ~2.8505 nS to ~67.2986 nS. Figure 4d illustrates the structure of the CNN containing two convolutional layers, two maximum-pooling layers, and a fully-connected layer. The detailed data flow in the CNN is described in Methods. After the CNN is properly trained by software which gives an accuracy baseline of 97.85%, the weights in convolutional kernel and fully-connected layer are quantized to 32 levels and transferred to flexible sliding ferroelectric synapses for subsequent edge inference task of MNIST handwritten-digit image recognition. Remarkably, the output maintains a high recognition accuracy of 97.81%, which is only a 0.04% loss compared to

Fig. 4 | Flexible sliding ferroelectric synapse. a Schematic of biological synapse. Signal transmission from the pre-synaptic terminal to the post-synaptic terminal is realized through ion channel by releasing neurotransmitters. **b** The synaptic weight PSC of a flexible SFeM versus gate pulse numbers, indicating the long-term potentiation and depression characteristics. **c** Cumulative probability of a flexible SFeM with respect to 32 independent drain-to-source conductance states. The conductance is programmed by applying different numbers of gate voltage pulses with 5 V amplitude and 10 ms width. **d** Structure of the five-layer CNN used for MNIST image recognition containing two convolutional layers (C1 and C2), two maximum-pooling layers (P1 and P2), and a fully-connected layer. The input is a 28 × 28 grayscale (8 bit) digit image. Bottom labels provide the feature map dimension (height × width × channel depth) or the vector dimension.

software baseline (Supplementary Fig. 16b). In addition, the high accuracy of handwritten-digit image recognition does not show obvious degradation over time (Supplementary Fig. 16b), indicating the superior retention and high fidelity of the edge inference results. Last but not least, other basic neuromorphic functions, such as the excitatory post-synaptic current, the paired-pulse facilitation, and the spike-timing dependent plasticity, are successfully demonstrated for the flexible SFeM devices (Supplementary Fig. 17), underscoring the great potential as a synaptic device.

Discussion

We demonstrate the room-temperature sliding ferroelectric non-volatile memories and synapses on both rigid and flexible substrates employing the as-grown inch-scale R-stacked bilayer MoS_2 as the device channel material. The SFeMs exhibit excellent performances, including a large memory window of >8 V, a high on/off conductance ratio of ~10^7, a long retention time of >10 years, and a programming endurance of over 10^4 cycles. Because of the remarkable flexibility afforded by the 2D nature, flexible SFeMs with state-of-the-art performances competitive to their rigid counterparts are achieved and can maintain their performances post-bending over 1000 cycles. Further, flexible sliding ferroelectric synapses which enable the emulation of specific Hebbian forms of long-term plasticity are demonstrated. Finally, we construct a five-layer CNN based on flexible sliding ferroelectric synapses and achieve an accuracy as high as 97.81% in the recognition of MNIST handwritten-digit images. Our work represents an important advancement in the field of 2D sliding ferroelectrics in terms of the realization of high-performance functional devices. Together with the unprecedented possibilities of on-demand design of atomically thin ferroelectrics (including ferroelectric semiconductors,

dielectric insulators, and even metals) facilitated by sliding ferroelectric mechanism, we anticipate that sliding ferroelectrics will promise the prospect of emerging technological applications in brain-inspired in-memory computing, neuromorphic computing, edge intelligence, and energy-efficient wearable electronics.

During the review of this article, we became aware of similar studies[58,59].

Methods

The growth of R-stacked bilayer MoS$_2$

Wafer-scale R-stacked bilayer MoS$_2$ is grown on single-crystal Ni (111) substrates by an interfacial epitaxy methodology[38]. Briefly, the transition metal Mo layer is first dissolved in 100-μm-thick single-crystal Ni (111) by annealing to form Ni−Mo alloy substrate. Next, a metal chalcogenide plate of ZnS is placed beneath the alloy to provide the chalcogen source. At the growth temperature (~770 °C), ZnS releases the S monomers that could dissolve into the Ni−Mo alloy substrate. The simultaneously dissolved sources are precipitated upward in the metal substrate, driven by both concentration and chemical potential gradient between the two surfaces of substrate. This results in the layer-by-layer interfacial epitaxy of R-stacked MoS$_2$ film.

Device fabrication and measurement

15 nm Ti (3 nm)/Au (10 nm)/Ti (2 nm) is patterned and deposited on silicon substrate as local back gate. Then, 20 nm Al$_2$O$_3$ is deposited by ALD as dielectric insulator at 200 °C using H$_2$O and trimethyl aluminum as precursors. Afterwards, the as-grown R-stacked bilayer MoS$_2$ is transferred from the growth substrate onto Al$_2$O$_3$ by using polydimethylsiloxane. Channel is then patterned by lithography and reactive ion etching. Contact electrodes are defined by lithography and 10 nm antimony (Sb) and 30 nm gold (Au) are finally deposited. Flexible devices share similar fabrication process where rigid Si substrates are replaced by flexible PET and the ALD temperature is lower to 150 °C and thickness of dielectric layer is 30 nm. All the patterning processes are done in an electron beam lithography system (Eline, Raith) with poly (methyl methacrylate) as photoresist and metal electrodes are deposited in a custom-built electron beam deposition system and followed by lift-off process. Electrical performances are measured in a custom-built probe station with semiconductor parameter analyzer (B1500A, Agilent) under a base pressure of 10^{-6} Torr at room temperature.

Optical and morphology characterization

Optical and morphology characterizations are conducted after the sample is transferred onto a rigid silicon substrate with 20-nm Al$_2$O$_3$ as the dielectric layer. Optical properties of the sample are characterized by SHG measurement and Raman spectroscopy. SHG is performed on a WITec alpha 300R system with a laser excitation wavelength of 1064 nm. Raman spectra are acquired using a HORIBA spectrometer (LabRAM HR Evolution) in a confocal backscattering configuration through a grating of 1800 gr/mm. Light from 532 nm (2.33 eV) continuous laser with a power of 137 μW for Raman measurements is focused through a Nikon objective (N.A. = 0.5, W.D. = 10.6, F.N. = 26.5) onto the sample with a spot diameter of ~ 2 μm. The spectrometer integration time is 30 s. Morphology characterization is carried out on an AFM (Cypher, Oxford instruments) under tapping mode, using the tip AC240TS-R3 (Oxford instruments).

PFM measurement

PFM measurements are conducted in situ on the epitaxy metal substrate using DART-SS-PFM mode to ensure strong signal-to-noise ratio on a commercial scanning probe microscope system (Cypher, Oxford instruments). DART stands for "Dual Amplitude Resonance Tracking", the SS stands for "Switching Spectroscopy". Antimony-doped and Pt/Ir-coated conductive silicon tips (SCM-PIT-V2, BRUKER) are utilized. The PFM hysteresis and loops are measured conducting on-off field switching technique. The external fields between tip and Ni during "on" stage switch the ferroelectric polarization of the sample while the piezoresponses are measured at "off" state where the field is canceled to avoid electrostatic effects.

STEM characterization

HAADF-STEM and STEM energy-dispersive X-ray spectroscopy (HAADF-STEM-EDX) are conducted on JEM-ARM200CF system (JEOL) operating at 200 kV. Samples for top-view stacking characterization are transferred onto a STEM grid. Samples for cross-section characterization and EDX analysis are cut from devices on silicon substrate by focused-ion-beam system (Helios 600I, FEI).

CNN simulation

A series of simulations are performed for the application of MNIST recognition. The simulator consists of a five-layer CNN. As depicted in Fig. 4d, the input is a 28 × 28 greyscale (8-bit) digit image. The first convolutional layer (C1) measuring 26 × 26 × 16 (weight × height × depth) is obtained after convolution with the 1 × 3 × 3 × 16 kernels (depth × weight × height × batch). The result is subsampled by a pooling layer (P1, 9 × 9 × 16) utilizing a 3 × 3 maximum-pooling operation with a sliding stride of 3. Subsequently, the second convolutional layer (C2, 7 × 7 × 32) is acquired with 32 stacked feature maps by a secondary convolution with the 16 × 3 × 3 × 32 kernels. This is followed by another round of subsampling, executed by another pooling layer (P2, 4 × 4 × 32) using a 2 × 2 maximum-pooling operation with a stride of 2. Ultimately, the expanded 512-element vector is applied to a fully-connected layer as an input, aiming to attain the computing result in accordance with the 10 probability outputs. The network training was completed by software with a 97.85% baseline accuracy. Throughout the course of these simulations, the measured data were normalized into [−1,1] according to its conductance range, and then replaced the 4-bit or 5-bit quantized weights in both kernel and FC layer. The accuracy over time is directly related to the change in device conductance value.

DFT calculations

We perform DFT calculations using the Vienna ab initio simulation package (VASP)[60,61] with the exchange-correlation potential described by the generalized gradient approximation and the Perdew−Burke−Ernzerhof functional[62]. We employ the projector augmented-wave method[63] and a plane-wave basis with kinetic energy cut-off of 520 eV. A Monkhorst-Pack k-mesh of 6 × 6 × 1 was adopted to sample the first Brillouin zone[64]. We used a vacuum layer of 21 Å to exclude the interactions from adjacent image layers, and applied a dipole correction along the z direction to correct the artificial electric polarization introduced by the periodic boundary condition. We calculated the DCD using VASPKIT package[65] by the difference between the total charge density of the bilayer and the superposition of the charge densities of two separate single layers, and the charge transfer was obtained as a planer integration of the DCD.

Data availability

Source data are provided with this paper and are available at https://doi.org/10.6084/m9.figshare.27316842.

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Author contributions

L.D. and G.Z. supervised the research project. X.L. and L.D. conceived the idea of constructing sliding ferroelectric memory on R-stacked bilayer MoS_2. X.L. carried out PFM measurements and device fabrication and measurement. B.Q. grown high-quality R-stacked MoS_2 samples and conducted SHG measurements under the supervision of C.L. and K.L., Y.W. and S.M. carried out the DFT calculation. Y.X. conducted CNN simulation under the supervision of J.T. Z.H. performed Raman spectra. Y.P. and C.C. contributed to device measurements. Z.P., J.Z., Z.C. and X.B. prepared TEM samples and carried out the measurements. M.Z. contributed to the schematics. D.S., N.L., W.Y. and R.Y. contributed to measurement setups. L.D., X.L. and G.Z. wrote the manuscript with the input from all authors.

Competing interests

The authors declare no competing interests.

Additional information

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